WE CLAIM:

1. A channel processor adapted for aligning a respective first hyper-concatenated data stream with a second hyper-concatenated data stream, each data stream being conveyed within a respective parallel channel and having substantially equivalent bit and frame rates, the channel processor being connected to a respective channel for processing the respective first data stream, and comprising:

   a) a framer adapted to detect incoming frames and generate a local strobe signal indicative of a timing of incoming frames of the respective first data stream;

   b) a memory for buffering incoming bits of the respective first data stream;

   c) an interface adapted to receive a master strobe signal from a selected adjacent channel processor; and

   d) an output timer adapted to control a position of a read pointer for outgoing bits of the respective first data stream based on a selected one of the local and master strobe signals.

2. A channel processor as claimed in claim 1, wherein the first and second hyper-concatenated data streams comprise concatenated Synchronous Optical Network (SONET) signals.

3. A channel processor as claimed in claim 1, wherein the parallel channels comprise any one or more of:

a) a wavelength of a Wave Division Multiplexed (WDM) or a Dense Wave Division Multiplexed (DWDM) optical communications system; and

b) a communications channel of a wireless communications system.

4. A channel processor as claimed in claim 1, wherein the framer comprises:

a) a detector circuit adapted to generate a detection signal indicative of detection of a selected byte of each incoming frame of the respective first data stream; and

b) a strobe circuit adapted to generate the local strobe signal with a predetermined timing relative to the detection signal.

5. A channel processor as claimed in claim 4, wherein the detector circuit is adapted to detect one or more of A1 and A2 bytes of incoming SONET frames, and to generate the detection signal with a predetermined timing relative to reception of the A1 byte.

6. A channel processor as claimed in claim 1, wherein the memory is a First-In-First-Out (FIFO) buffer having a read pointer indicative of an address of an outgoing bit of the respective first data stream.

7. A channel processor as claimed in claim 6, wherein a storage capacity of the memory is selected on a basis of a maximum anticipated misalignment between the first and second data streams.

8. A channel processor as claimed in claim 7, wherein the storage capacity of the memory is equivalent to at most about one-half of a data frame.

9. A channel processor as claimed in claim 7, wherein the storage capacity of the memory is equivalent to a number of bits received during a time interval of at most about 250 nano-seconds (nSec).

10. A channel processor as claimed in claim 6, wherein the output timer comprises:

a) a phase error detector adapted to detect a phase error between the local strobe signal and the master strobe signal; and

b) a pointer adjustment circuit adapted to adjust the read pointer based on the detected phase error.

11. A channel processor as claimed in claim 6, wherein the output timer comprises a program-controlled circuit adapted to measure a phase error between the local strobe signal and the master strobe signal, and adjust the read pointer based on the measured phase error.

12. A channel processor as claimed in claim 10, wherein the phase error detector comprises a counter adapted to count a number of clock pulses between the local strobe signal and the master strobe signal.

13. A channel processor as claimed in claim 10, further comprising an offset circuit adapted to apply a predetermined offset to the read pointer.

14. A channel processor as claimed in claim 13, wherein the predetermined offset is selected to compensate for a propagation delay of the master strobe signal.

15. A channel processor as claimed in claim 10, wherein the output timer further comprises a switch circuit adapted to supply a selected one of the local strobe signal and the master strobe signal to an input of the phase error detector, such that the phase error detector can be selectively controlled to detect one of: a phase error between the local strobe signal and the master strobe signal; and a phase error between the local strobe signal at first and second inputs.

16. A channel processor as claimed in claim 1, wherein the interface comprises first and second input circuits adapted to receive a master strobe signal from a respective one of the first and second adjacent channel processors.

17. A channel processor as claimed in claim 16, further comprising a direction selector circuit adapted to couple a selected one of the first and second input circuit to the output timer, such that a master strobe signal propagated from a direction of the selected adjacent channel processor can be used by the output timer.

18. A channel processor as claimed in claim 16, wherein the interface further comprises first and second output circuits adapted to send a selected one of the local strobe signal and the master strobe signal to a respective one of the first and second adjacent channel processors.

19. A system for processing a plurality of data streams, each data stream being conveyed within a respective parallel channel of a communications network and at least two of the data streams being hyper-concatenated data streams, the system comprising a plurality of parallel channel processors, each channel processor comprising:

a) a framer adapted to generate a local strobe signal indicative of a timing of incoming frames of a respective data stream;

b) a memory for buffering incoming bits of a respective data stream;

c) an interface adapted to receive a master strobe signal from a selected adjacent channel processor; and

d) an output timer adapted to control a position of a read pointer for outgoing bits of the respective data stream based on a selected one of the local and master strobe signals.

20. A system as claimed in claim 19, further comprising a control unit adapted to:

a) designate a master channel processor to operate in a free-running mode in which the timing of outgoing bits of a respective master hyper-concatenated data stream is based on the respective local strobe signal; and

b) designate a slave channel processor to operate in a slave mode in which the timing of outgoing bits of a respective slave hyper-concatenated data stream is synchronized to that of the master data

stream based on a master strobe signal originating from the master channel processor.

21. A system as claimed in claim 19, wherein each channel processor is further adapted to selectively propagate a strobe signal received from one adjacent channel processor to an opposite adjacent channel processor.

22. A system as claimed in claim 21, wherein the control unit is further adapted to control a set of two or more adjacent slave channel processors to successively propagate a strobe signal originating from the master channel processor to each one of the set of adjacent slave channel processors, whereby the timing of outgoing bits of each respective slave data stream is synchronized with that of the master data stream.

23. A system as claimed in claim 19, wherein each of the master and slave data streams comprise concatenated Synchronous Optical Network (SONET) signals.

24. A system as claimed in claim 19, wherein the parallel channels comprise any one or more of:

a) a wavelength of a Wave Division Multiplex (WDM) or a Dense Wave Division Multiplex (DWDM) optical communications system; and

b) a communications channel of a wireless communications system.

25. A system as claimed in claim 19, wherein the framer comprises:

a) a detector circuit adapted to generate a detection signal indicative of detection of a first byte of each incoming frame of the respective data stream; and

b) a strobe circuit adapted to generate the local strobe signal with a predetermined timing relative to the detection signal.

26. A system as claimed in claim 25, wherein the detector circuit is adapted to detect one or more of A1 and A2 bytes of incoming SONET frames, and to generate the detection signal at a timing of reception of the A1 byte.

27. A system as claimed in claim 19, wherein the memory is a First-In-First-Out (FIFO) buffer having a read pointer indicative of an address of a successive outgoing bit of the respective data stream.

28. A system as claimed in claim 27, wherein a storage capacity of the memory is selected on a basis of a maximum anticipated misalignment between data streams received by the signal processor.

29. A system as claimed in claim 28, wherein the storage capacity of the memory is equivalent to at most about one-half of a data frame.

30. A system as claimed in claim 28, wherein the storage capacity of the memory is equivalent to a number of bits received during a time interval of at most about 250 nano-seconds (nSec).

31. A system as claimed in claim 27, wherein the output timer comprises:

a) a phase error detector adapted to detect a phase error between the local strobe signal and the received strobe signal; and

b) a pointer adjustment circuit adapted to apply a first offset to the read pointer based on the detected phase error.

32. A system as claimed in claim 31, wherein the phase error detector comprises a counter adapted to count a number of clock pulses between the local strobe signal and reception of the master strobe signal.

33. A system as claimed in claim 31, wherein the output timer further comprises an offset circuit adapted to apply a predetermined offset to the read pointer.

34. A system as claimed in claim 33, wherein the predetermined offset is selected to compensate a propagation delay of the master strobe signal.

35. A system as claimed in claim 31, wherein the output timer further comprises a switch circuit adapted to supply a selected one of the local strobe signal and the master strobe signal to an input of the phase error detector, such that the phase error detector can be selectively controlled to detect either: a phase error between the local strobe signal and the received strobe signal; or a phase error between the local strobe signal and itself.

36. A system as claimed in claim 19, wherein the interface comprises first and second input circuits adapted to receive a master strobe signal from a respective one of the first and second adjacent channel processors.

37. A system as claimed in claim 36, further comprising a direction selector circuit adapted to couple a selected one of the first and second input circuit to the output timer, such that a master strobe signal propagated from a direction of the selected adjacent channel processor can be used by the output timer.

38. A system as claimed in claim 36, wherein the interface further comprises first and second output circuits adapted to send a selected one of the local strobe signal and the master strobe signal to a respective one of the first and second adjacent channel processors.

39. A method of processing two or more hyper-concatenated data streams, each data stream being conveyed within respective adjacent parallel channels of a communications network, the method comprising steps of:

a) designating a one of the hyper-concatenated data streams as a master data stream;

b) designating all others of the hyper-concatenated data streams as slaves to the master;

c) at a channel processor for the master data stream, generating a master strobe signal;

d) propagating the master strobe signal to respective channel processors of each one of the slave data streams; and

e) at the respective channel processor for each slave data stream, adjusting a respective read pointer for outgoing bits of the respective data stream, using a local strobe signal and the master strobe signal.

40. A method as claimed in claim 39, wherein the step of propagating the master strobe signal comprises a step of passing the master strobe signal from the master channel processor to an adjacent slave channel processor.

41. A method as claimed in claim 40, wherein the step of propagating the master strobe signal further comprises a step of passing the master strobe signal to each successive adjacent slave channel processor in a direction away from the master channel processor.

42. A method as claimed in claim 39, wherein each of the hyper-concatenated data streams comprise concatenated Synchronous Optical Network (SONET) signals.

43. A method as claimed in claim 39, wherein the step of generating the master strobe signal comprises the steps of:

a) generating a detection signal indicative of detection of a first bit of each incoming frame of the respective master data stream; and

b) generating the master strobe signal with a predetermined timing relative to the detection signal.

44. A method as claimed in claim 43, wherein the step of generating a detection signal comprises the steps of detecting one or more of A1 and A2 bytes of incoming frames; and generating the detection signal with a predetermined timing relative to a first bit of the A1 byte.

45. A method as claimed in claim 39, wherein the step of adjusting a read pointer for outgoing bits of the respective slave data stream comprises the steps of :

a) detecting a phase error between a local strobe signal and the master strobe signal; and

b) adjusting the read pointer based on the detected phase error.

46. A method as claimed in claim 45, wherein the local strobe signal is generated by:

a) generating a detection signal indicative of detection of a first bit of each incoming frame of the respective slave data stream; and

b) generating the local strobe signal at a predetermined timing relative to the detection signal.

47. A method as claimed in claim 46, wherein the step of generating a detection signal comprises the steps of detecting one or more of A1 and A2 bytes of incoming frames of the slave data stream; and generating the

detection signal with a predetermined timing relative to a first bit of the A1 byte.

48. A method as claimed in claim 45, wherein the step of detecting a phase error comprises a step of counting a number of clock pulses between the local strobe signal and reception of the master strobe signal.

49. A method as claimed in claim 45, wherein the step of adjusting the read pointer for outgoing bits of the respective slave data stream further comprises a step of applying a predetermined offset to the read pointer.

50. A method as claimed in claim 49, wherein the predetermined offset is selected to compensate a propagation delay of the master strobe signal.

51. A method as claimed in claim 45, wherein the step of adjusting the read pointer of outgoing bits of the respective slave data stream further comprises a step of supplying a selected one of the local strobe signal and the master strobe signal to an input of a phase error detector, such that the step of detecting a phase error is selectively controlled to comprise a step of either one of: detecting a phase error between the local strobe signal and the master strobe signal; and detecting a phase error between the local strobe signal and itself.

52. A method of transporting a high-bandwidth signal comprising M hyper-concatenated data streams across a network between a source node and a destination node, the method comprises the steps of:

a) providing an end-to-end path between the source node and the destination node, the end-to-end path comprising at least M parallel channels;

b) launching each data stream from the source node toward the destination node through respective ones of the channels;

c) aligning each of the data streams at a downstream end of each hop toward the destination node; and

d) reassembling the high-bandwidth signal at the destination node.